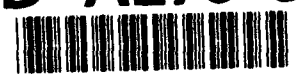

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Final Report
Grant No. N00014-91-P-2037
PR No. 68-5154-92

Research on High Reliability Refractory Ohmic Contacts for GaAs FETs and MODFETs

Submitted to:

Dr. W. T. Anderson
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SEAS Report No. UVA/525469/EE94/101
February 1994

DEPARTMENT OF ELECTRICAL ENGINEERING

SCHOOL OF
ENGINEERING
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University of Virginia
Thornton Hall
Charlottesville, VA 22903

UNIVERSITY OF VIRGINIA
School of Engineering and Applied Science

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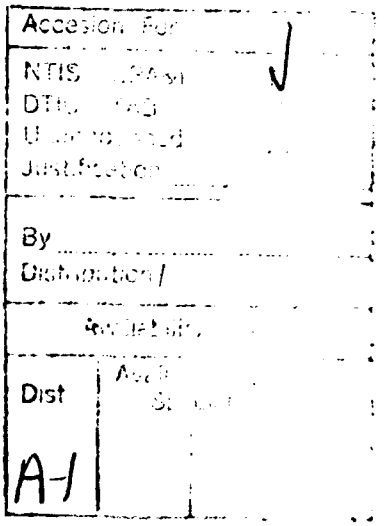

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High temperature characteristics of amorphous $TiWSi_x$ nonalloyed ohmic contacts to GaAs

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This article reports on amorphous (α) nonalloyed $TiWSi_x$ ohmic contacts on n-GaAs using an intervening graded-band-gap layer of $In_xGa_{1-x}As$ grown by the low pressure organometallic chemical vapor deposition method. The metal silicide contacts consisted of extremely thin alternating layers of TiW and Si sequentially deposited by rf magnetron sputtering to a total thickness of 500 Å. The as-deposited contacts exhibited ohmic behavior without requiring post-deposition heat treatment, and yielded specific contact resistivity values as low as 9×10^{-7} Ω cm^2. These contacts were shown to be stable and retained excellent surface morphology after 600 °C thermal annealing. Rutherford backscattering and Auger electron spectroscopy investigations revealed no apparent interdiffusion at the metal/semiconductor interface under the above annealing conditions.

I. INTRODUCTION

Gallium arsenide based field-effect transistors (FETs), high electron mobility transistors (HEMTs), heterojunction bipolar transistors (HBTs), and monolithic microwave integrated circuits (MMICs) require ohmic contacts with two important features: (a) low parasitic resistance for improved gain and noise performance and (b) stable metal contact technology for high reliability and high temperature applications. Conventional Au and Ag based ohmic contact systems on GaAs[1] i.e., AuGe, AuGe/Ni for n-type and AuGe, AuZn, AgZn for p type, suffer from a number of drawbacks. First, they are unstable above 300 °C, thus limiting their use for long term high temperature applications. Second, they require alloying between 350 and 450 °C which leads to nonuniformity, poor reproducibility, and loss of dimensional control. In addition, the alloying process involves liquid phase reactions at the metal/semiconductor interface which result in a rough surface morphology and metal (Ni or Au) diffusion into the adjacent layers.[2] In order to alleviate these problems, a number of nonalloyed contact systems to GaAs have been proposed. Woodall *et al.*[3] utilized the fact that the Fermi level pinning for InAs occurs in the conduction band, thus producing a nonalloyed ohmic structure with a nearly zero Schottky barrier height. Using molecular beam epitaxy (MBE)-grown $In_xGa_{1-x}As$ graded-band-gap layers on GaAs and Ag metallization, they achieved nonalloyed ohmic contact resistivities in the range 5×10^{-7}–5×10^{-6} Ω cm^2. Ohmic contacts to MBE-grown graded-gap InGaAs/GaAs using W metallization have also been demonstrated[4] yielding specific contact resistivity values of 1×10^{-5} Ω cm^2. Similarly, thermally stable ohmic contacts to n-GaAs were produced[5,6] by introducing a thin interfacial layer of $In_xGa_{1-x}As$ between the GaAs and the metallization by In-Ga interdiffusion from a refractory-metal/In metallization deposited on GaAs.

This work is focused on the investigation of refractory ohmic contact metallizations for GaAs, AlGaAs, and InGaAs structures for high temperature, high reliability applications using a combination of amorphous metal silicide films of $TiWSi_x$ and low-pressure organometallic chemical vapor deposition (LPOMCVD)-grown graded-band-gap $In_xGa_{1-x}As$ layers. The amorphous $TiWSi_x$ multilayered system was selected because it was previously[7,8] shown, along with WSi_x, to be a stable gate metallization on GaAs and InP. In addition, WSi_x and $TiWSi_x$ are effective diffusion barriers which prevent chemical interfacial reactions and greatly reduce interdifusion at the metal-semiconductor interface.

II. EXPERIMENTAL RESULTS

A. Contact fabrication

The epitaxial layers were grown on (100) undoped GaAs substrates misoriented 2° toward the (110). The schematic cross section of the contact structure studied is shown in Fig. 1 and consisted of a 0.5 μm undoped GaAs buffer layer, a 2000 Å n-GaAs layer doped at 2×10^{17} cm^{-3}, a 500 Å n^+-GaAs layer doped at 3×10^{18} cm^{-3}, a $In_xGa_{1-x}As$ n-doped (3×10^{18} cm^{-3}) layer which was graded in composition from $x=0.1$ to $x=0.6$, and finally a 100 Å n^+-$In_xGa_{1-x}As$ capping layer doped at 3×10^{18} cm^{-3}. Contact structures containing either $In_{0.5}GaAs_{0.5}$ or InAs capping layers were investigated. The source materials for the epitaxy included trimethylindium (TMI), trimethylgallium (TMG), and arsine. Typical LPOMCVD process parameters included: reactor temperatures between 550 and 675 °C, reactor pressure of 0.1 atm, TMG mole fractions between 0 and 1×10^{-4}, TMI mole fractions between 0 and 7×10^{-5}, and total gas flow of 8 ℓ/min. Silane (SiH_4) was used to dope both the GaAs and the $In_xGa_{1-x}As$. The composition of the graded-$In_xGa_{1-x}As$ was estimated from photoluminescence spectra of uniform

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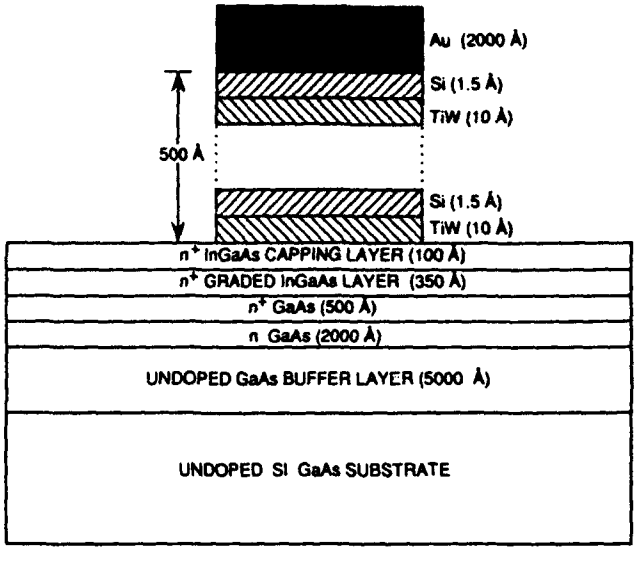

FIG. 1. Schematic cross section of the LPMOCVD-grown graded-InGaAs ohmic contact structure and the multilayered TiW/Si metallization system.

composition $In_xGa_{1-x}As/GaAs$ heterostructures and Auger analysis of the actual graded structures. Silicon doping concentrations were determined using the capacitance-voltage (C-V) profiling technique. Following the epitaxial growth, ohmic contact test patterns were fabricated using a standard photolithographic and lift-off process. A second photolithographic step was used to isolate around the test patterns to a depth of 5000 Å. The $TiWSi_x$ amorphous refractory metallization consisted of alternating layers of TiW (10 Å) and Si (1.5 Å) deposited to a total thickness of 500 Å by a rf magnetron sputtering technique. The TiW target was fabricated from pressed powder which had a 20 at. % Ti and 80 at % W composition. The sputtering system has a power splitting capability and substrate stage rotation. By adjusting the power delivered to the individual target and the speed of sample rotation, precise control of the composition of the amorphous metallization was achieved.[9] With a sputtering pressure of 8×10^{-3} Torr of Ar gas, a total rf power of 500 W and 5 rpm stage rotation, deposition rates of 50 Å/min and 7.5 Å/min were obtained for TiW and Si, respectively. This method has the advantage that the substrate, as it rotates, spends only a small fraction of time under the sputter target, and the surface of the sample remains at relatively low temperatures thus facilitating the photoresist lift-off process. As shown previously,[10] alternating layers with sputter deposited Si and TiW result in an amorphous layer. Subsequent to the $TiWSi_x$ sputter deposition, a 2000-Å-thick Au overlay was deposited by an e-beam evaporation method; finally the metal was lifted-off in acetone. For the purpose of comparison, e-beam deposited conventional AuGe (800 Å)/Ni(200 Å)/Au(1500 Å) ohmic contact metallizations were also investigated.

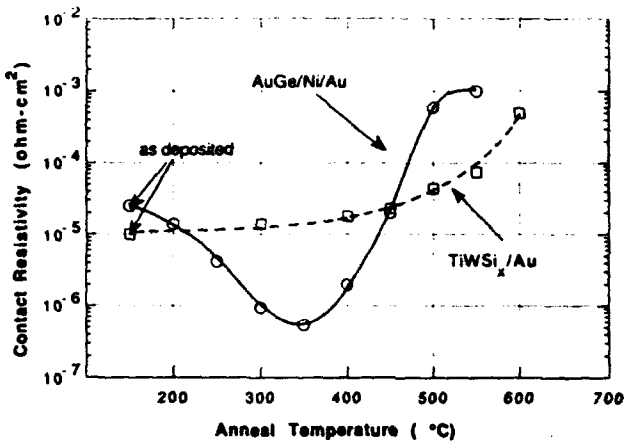

FIG. 2. Contact resistivity of $TiWSi_x$ (500 Å)/Au (2000 Å) and AuGe (800)Å/Ni (200)Å/Au (2000)Å metallization on $In_{0.5}Ga_{0.5}As$/graded-$In_xGa_{1-x}As/GaAs$ structure as a function of anneal temperature with 2 min anneal cycle in forming gas.

B. Electrical characterization

Specific contact resistivity measurements were made using a test pattern conforming to the transmission line model (TLM) as described by Reeves *et al.*[11] with 200 μm$\times$200 μm contact windows and spacings ranging from 5 to 50 μm. The specific contact resistivity (ρ_c) values were obtained from the so-called "transfer length" (L_T) measurements under the assumption that the sheet resistance under the contact is equal to the sheet resistance between the contacts. This assumption is justified in our case since, due to the refractory nature of the $TiWSi_x$, no alloying or sintering occurs at the metal-semiconductor interface and thus no modification of the sheet resistance takes place under the contact as a result of thermal treatment. It is therefore possible to obtain correct values of the specific contact resistivity without the need of contact end resistance measurements. Although both the AuGe/Ni and

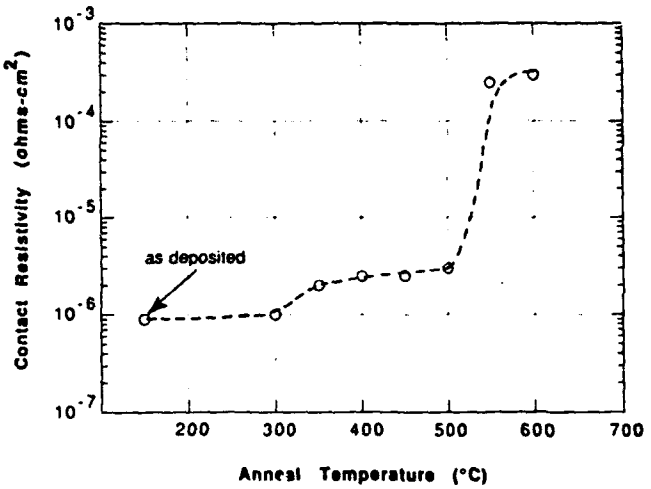

FIG. 3. Contact resistivity of $TiWSi_x$ (500)/Au (2000 Å) contact metallization on InAs/graded-$In_xGa_{1-x}As/GaAs$ structure as a function of anneal temperature with 2 min anneal cycle in forming gas.

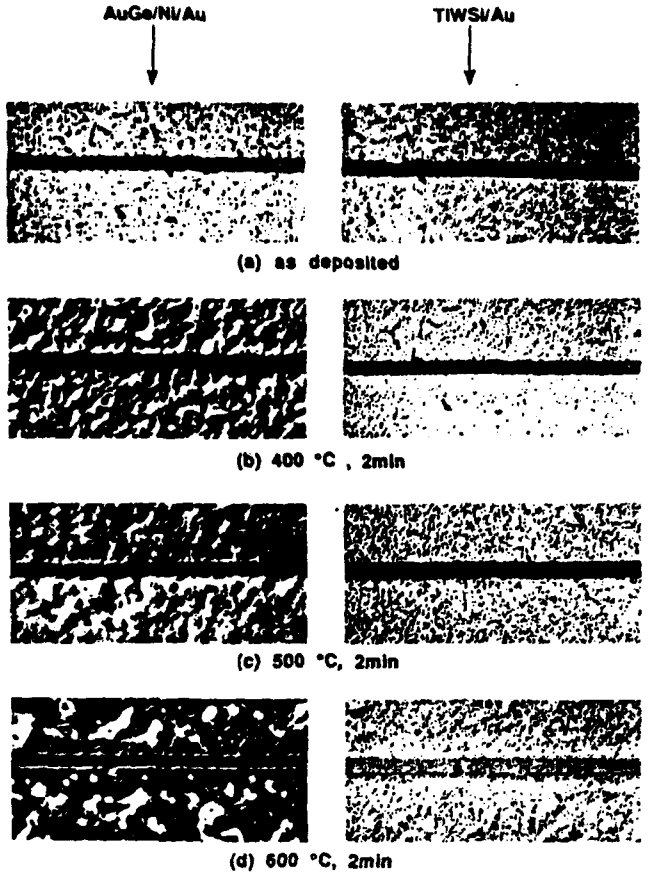

FIG. 4. Optical micrographs showing the surface morphology of $TiWSi_x$ (500 Å)/Au (2000 Å) and AuGe (800 Å)/Ni (200 Å)/Au (2000 Å) ohmic metallizations before and after annealing at 400, 500, and 600 °C for 2 min.

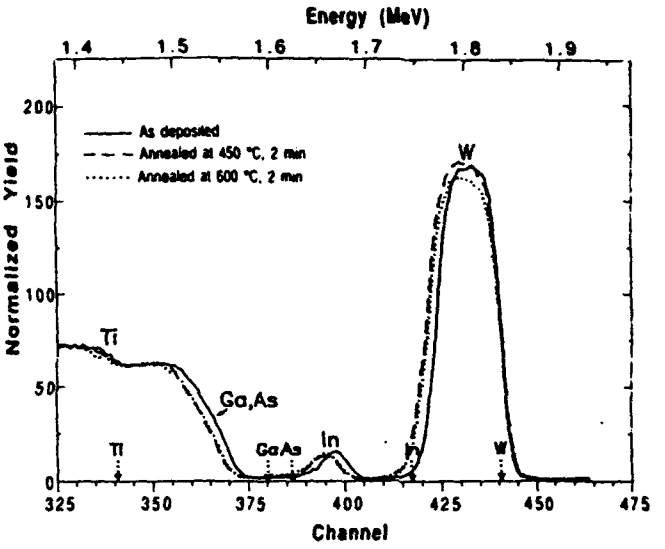

FIG. 5. 2 MeV Rutherford backscattering spectra for $TiWSi_x$ on $In_{0.5}Ga_{0.5}As$/GaAs before and after 2 min annealing at 450 and 600 °C.

$TiWSi_x$ metallizations exhibited excellent ohmic contact characteristics without the need of heat treatment, the metallizations were subjected to thermal annealing in order to investigate their thermal stability. Annealing of the layered films was carried out in the 200–600 °C range on a strip heater for 2 min in a forming gas ambient. Both the as-deposited $TiWSi_x$ and AuGe/Ni contacts on the $In_{0.5}Ga_{0.5}As$/graded-$In_xGa_{1-x}As$/GaAs structure exhibited ohmic type behavior. Figure 2 shows plots of the contact resistivity of $TiWSi_x$/Au and AuGe/Ni/Au metallizations on $In_{0.5}Ga_{0.5}As$/graded-InGaAs/GaAs as a function of anneal temperature. The typical contact resistivity for the as-deposited AuGe/Ni/Au metallization is about 2.5×10^{-5} Ω cm^2. Upon annealing, the contact resistivity decreases with temperature and exhibits a minimum at about 350 °C indicating the onset of interfacial liquid phase reactions which occur at the AuGe eutectic temperature of 356 °C. Further annealing causes a large increase, by two orders of magnitude, in the contact resistivity from 400 to 550 °C. The companion $TiWSi_x$/Au contact typically has as-deposited contact resistivity of 1×10^{-5} Ω cm^2 and remains rather unchanged up to 450 °C. A similar plot of the contact resistivity for the $TiWSi_x$/Au metallization on an InAs/graded InGaAs/GaAs structure as a function of anneal temperature is shown in Fig. 3. This plot reflects similar contact behavior as with that of the corresponding plot of Fig. 2, except that the as-deposited value of the contact resistivity is about a factor of 10 lower indicating a reduction in the contact resistivity as the mole fraction of In concentration in the capping layer increases. In this case, the contact resistivity for the as-deposited $TiWSi_x$/Au contacts is measured at 9×10^{-7} Ω cm^2 with only a slight increase in the 300–500 °C temperature range and increasing abruptly beyond 500 °C.

C. Surface morphology

Optical micrographs of both $TiWSi_x$/Au and AuGe/Ni/Au contact metallizations before and after annealing are shown in Fig. 4. The AuGe/Ni/Au contacts begin to show surface texturing at temperatures as low as 400 °C as a result of melting at the AuGe eutectic temperature. Above 400 °C the degradation of the surface becomes even more severe as the AuGe alloys with the semiconductor. Formation of a liquid phase in the AuGe/Ni alloying process leads to the roughening of the contact border and results in poor edge definition. As indicated earlier, extensive alloying also resulted in the degradation of the electrical characteristics of the AuGe/Ni/Au contacts. By comparison, the amorphous $TiWSi_x$/Au contacts showed very little surface modification as a result of 400, 500, and 600 °C, 2 min thermal anneals. The surface morphology remains smooth and excellent edge definition is maintained up to 600 °C. In fact, the very minor changes observed in the $TiWSi_x$/Au surface structures were attributed to reactions in the the Au overlayer rather than the $TiWSi_x$/InGaAs contact interface itself. This was particularly evidenced when observing annealed $TiWSi_x$ films which did not have the Au overlay. It is believed that a small amount of AuSi eutectic is formed above 600 °C at the Au/$TiWSi_x$ interface.

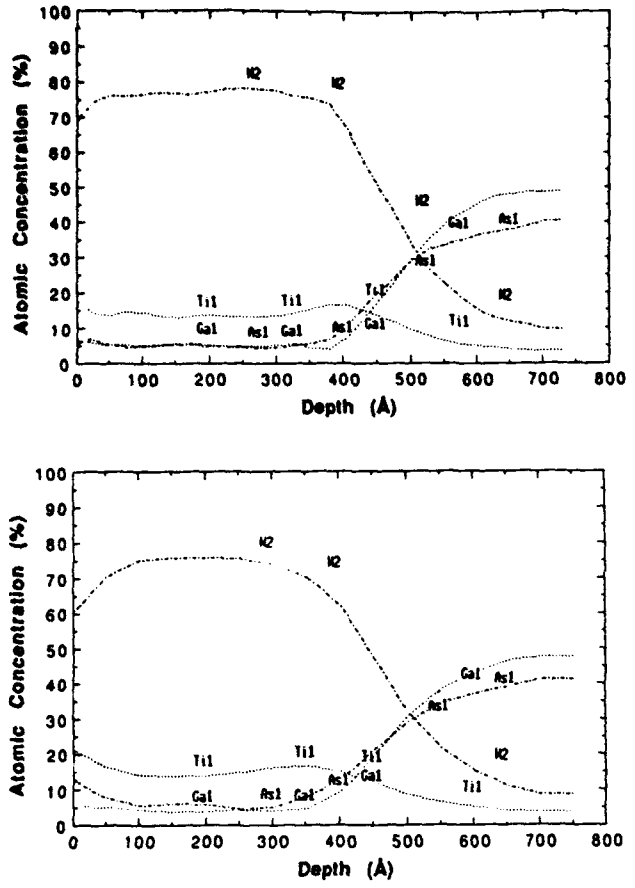

FIG. 6. AES profiles of $TiWSi_x$ on $In_{0.5}Ga_{0.5}As$/graded-InGaAs/GaAs structure (a) as-deposited (b) after annealing at 600 °C for 2 min in forming gas ambient.

D. RBS and AES analyses

Metallurgical reactions at the $TiWSi_x$/semiconductor interface were investigated with 2 MeV $^4He^{++}$ Rutherford backscattering spectroscopy (RBS). The RBS spectra for samples before and after annealing are shown in Fig. 5. These spectra reveal that no significant interdifusion of the contact interface occurred as a result of 450 and 600 °C anneals. The slight shift of the RBS spectrum that can be observed for the as-deposited sample is attributed to small variations in the $TiWSi_x$ thickness. The stability of the $TiWSi_x/In_{0.5}Ga_{0.5}As$ interface was also investigated by Auger electron spectroscopy (AES). The AES spectra were obtained using a scanning auger microprobe (SAM) with 10 keV, 200 μA primary electron beam and a spot size of 0.1 μm. The depth profiles were acquired by monitoring the depth distribution of all the related elements, i.e., W, Ti, Ga, and As. Figure 6 shows the AES profiles for the $TiWSi_x/In_xGa_{1-x}As$ structure before [Fig. 6(a)] and after [Fig. 6(b)] annealing at 600 °C for 2 min in forming gas. It is seen that there is only a very slight reduction in the sharpness of the interface as a result of the annealing treatment. The profiles do not show significant broadening of the $TiWSi_x$/InGaAs interface which would have been indicative of interdiffusion.

III. CONCLUSION

In conclusion, ohmic contacts to *n*-GaAs using graded-band-gap layers of LPMOCVD-grown $In_xGa_{1-x}As$ and sputter-deposited amorphous $TiWSi_x$ films were investigated. The as-deposited contacts exhibited contact resistivity values of 1×10^{-5} Ω cm^2 and 9×10^{-7} Ω cm^2 for $In_{0.5}Ga_{0.5}As$ and InAs caps, respectively. In general, these contacts remained electrically stable and maintained excellent surface morphology up to 500 °C. Initial RBS and AES analyses have not revealed significant interdiffusion at the silicide/semiconductor interface up to 600 °C. In contrast, conventional AuGe/Ni metallizations exhibited morphology and contact resistivity degradation above 400 °C.

ACKNOWLEDGMENTS

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All-Refractory GaAs FET Using Amorphous $TiWSi_x$ Source/Drain Metallization and Graded-$In_xGa_{1-x}As$ Layers

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Abstract— We report on the fabrication of an all-refractory GaAs field-effect transistor having non-alloyed source and drain ohmic contacts and a TiW/Au refractory gate metallization. The ohmic contacts consist of amorphous $TiWSi_x$ metallization and intervening graded InGaAs layers grown by low pressure organometallic vapor phase epitaxy (LPOMVPE). The amorphous $TiWSi_x$ is formed using alternating layers of TiW(10 Å) and Si(1.5 Å) deposited by an RF magnetron sputtering technique. The resulting all-refractory FET devices exhibited excellent dc transistor characteristics with measured transconductance of 140 mS/mm. The dc performance of these devices was comparable to conventional devices with AuGe/Ni/Au contacts fabricated using similar material structures.

I. Introduction

ENHANCED reliability and high temperature operation of discrete GaAs MESFET's (or FET's) [1] as well as GaAs monolithic microwave integrated circuits (MMIC's) [2] and digital integrated circuits [3] have already been achieved by using a refractory-metal gate electrode. The superior thermal stability of TiW, WSi, TiWSi [4]–[6], or TiWN [2] gate metallizations prevent the interdiffusion of Au from the overlays into the active regions of the devices thus maintaining the integrity of the rectifying Schottky gates. In addition, the robustness of these refractory gate materials helps in reducing electromigration and enhances device reliability [7]. The utilization of refractory metals for the gate material is natural since they guarantee abrupt metal–semiconductor interfaces and prevent alloying or interdiffusion at elevated temperatures. In contrast to the rectifying gate metallizations, the source and drain contacts must be ohmic and, in the standard technology, require alloying of the metal–semiconductor interfaces. Presently, AuGe based eutectic ohmic contacts are widely employed for n-GaAs in the fabrication of MESFET's, HEMT's and HBT's. The inherent thermal instability of these contacts allows for relatively low alloying temperatures (350–430° C) and produces low resistivity ohmic contacts. However, the alloying process, which involves liquid phase reactions at the metal-semiconductor interface, leads to rough surface morphology, degraded edge profiles and deep interdiffusion which adversely affect the reliability of the devices [8]. Hence, a refractory drain and source metallization system is needed which is thermally stable and reliable, yet ohmic to n-GaAs.

As demonstrated by Woodall *et al.* [9], nonalloyed ohmic contacts to n-GaAs can be realized by using an intervening layer of graded-InGaAs between the metal and the GaAs. The low resistivity nonalloyed ohmic behavior of these contacts is generally independent of the type of metal used because the metal-$In_xGa_{1-x}As$ barrier height becomes negative when the Indium concentration (x) exceeds 70% [9], [10]. HEMT's with non-alloyed ohmic contacts using n^+ InGaAs cap layers and Al source/drain and gate metallizations have been reported [11]. Recently, low resistivity refractory non-alloyed ohmic contacts to n-GaAs have been achieved using W [12] and $TiWSi_x$ [13] metallizations in combination with an appropriate intervening layer of graded-InGaAs. In this letter we describe the fabrication and characterization of 1-μm-gate length GaAs FET's which employ a refractory TiW gate metallization and amorphous $TiWSi_x$ drain and source ohmic contacts deposited on a graded-InGaAs/GaAs structure.

II. Experimental Procedure

A schematic of the FET layered structure is shown in Fig. 1. The graded-InGaAs/GaAs epitaxial layers were grown on (100) undoped GaAs substrates misoriented 2° toward the (110), using low pressure organometallic vapor phase epitaxy (LPOMVPE). The structure consists of 0.5-μm n^- buffer layer, a 2000-Å thick n (2×17 cm^{-3}) active layer, a 500 Å $n^+ - GaAs$ layer, and a 500 Å graded $n^+ - In_xGa_{1-x}As$ layer ($0 \le x \le 1$), with the surface being terminated in InAs ($x = 1$). The growth parameters include trimethygallium mole fractions between $0 - 1 \times 10^{-4}$, trimethylindium mole fractions between $0 - 0.7 \times 10^{-4}$, *V/III* ratios of 50–100, total gas flow rates of 8.2 *l*/min, and a reactor pressure of 0.1 atm. The graded-$In_xGa_{1-x}As$ capping layer and the GaAs buffer layers are grown at 600° C, while the active n/n^+ FET layers were grown at 675° C.

Device fabrication begins with a 2500-Å deep mesa wet etch, followed by photoresist patterning of the source and drain contacts. The amorphous $TiWSi_x$ metallization is sputter-deposited; a Au (1000 Å) layer is then e-beam deposited and the metal subsequently lifted-off. Details of the ohmic contact formation and characterization were reported previously [12].

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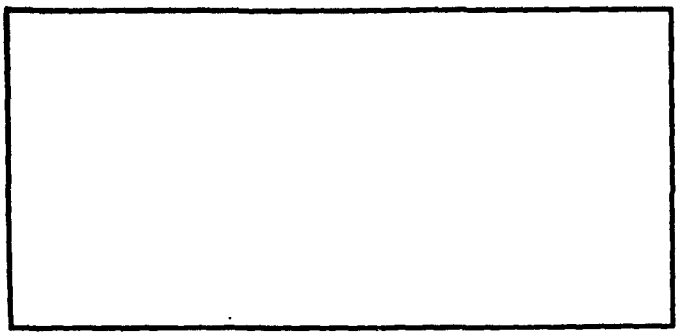

Fig. 1. Schematic cross section of the all-refractory FET layered structure.

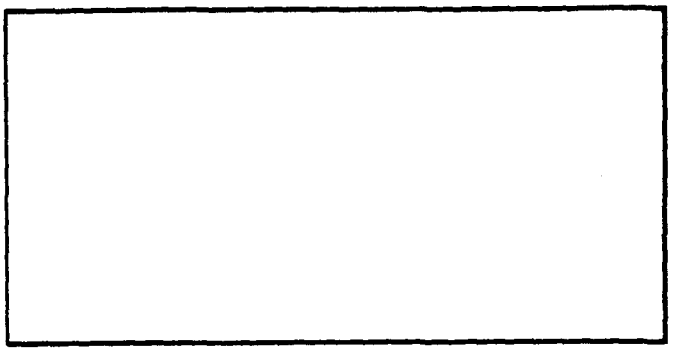

Fig. 2. Specific contact resistance of the $TiWSi_x$/graded-InGaAs/GaAs ohmic contacts as a function of anneal temperature for 2-min anneals.

The amorphous $TiWSi_x$ metallization consists of alternating layers of TiW (10 Å) and Si(1.5 Å) deposited to a total thickness of 500 Å by an RF magnetron sputtering technique. The multilayered metallization is obtained by rotating the sample under both TiW (10 wt% Ti-90 wt% W) and Si targets during the sputtering process. After the gate photolithography is completed, the graded-InGaAs and n^+ – GaAs layers are etched away in (1:1:80) H_2SO_4: H_2O_2: H_2O solution exposing the n active layer prior to the gate metallization. A TiW(500 Å)/Au(2000 Å) gate metallization is formed by an e-beam evaporation [4] and lift-off process. Fabrication is concluded with Ti/Au overlay formation using another photolithography and lift-off step. Both standard FET's and T-gate FET's with gates 1-μm long and 250-μm wide were fabricated.

The contact resistivity measurements were made using the transmission line model (TLM) method as described by Reeves and Harrison [14] under the assumption that the sheet resistivity under the contacts is the same as that between them. This assumption is justified in this case, since alloying or sintering at the metal semiconductor interface is not expected to occur due to the refractory nature of the metallization. As reference devices, we also fabricated conventional FET's with identical geometries and layered structures as those used in the all-refractory devices; the graded $In_xGa_{1-x}As$ contact layer was omitted from these structures. These control devices utilized standard AuGe/Ni/Au metallization for source/drain ohmic contacts which were annealed at 410° C for 1 min.

III. Results

The as deposited $TiWSi_xAu$ contacts exhibited ohmic type behavior and without the need for alloying or any other thermal treatment. The thermal stability of the contacts was investigated under high temperature annealing conditions carried out in the 200–600° C temperature range on a strip heater in forming gas ambient for 2-min cycles. The results which are shown in Fig. 2 represent the specific contact resistivity of the $TiWSi_x$ graded-InGaAs/GaAs contacts as a function of anneal temperature. The as deposited contacts were ohmic with contact resistivities of 1×10^{-6} ohm-cm^2 which remains relatively constant up to 300° C, followed by a small increase, up to 1.2×10^{-6} ohm·cm^2, in the temperature range between 300° C and 500° C. However, beyond 500° C a more severe degradation of the electrical properties is observed as evidenced by a rapid increase in the contact resistivity which reaches a maximum value of 3.0×10^{-4} ohm·cm^2 after a 600° C, 2-min anneal. In addition, the surface morphology of the $TiWSi_x$/graded-InGaAs contacts, as determined by Nomarsky interference microscopy, is very stable with little modification occurring as a result of the 400° C, 500° C, and 600° C anneals. The surface remains smooth, and excellent edge definition is maintained up to 600° C. The devices were well-isolated with device-to-device leakage currents that were in the range of a few nanoamperes for bias voltages of 5 V.

The gate–source Schottky diodes exhibit a drain–source breakdown voltage of −9.5 V, defined at I_D = 2 mA/mm (10% of the I_D at peak transconductance). The gate reverse saturation current was 15 nA at 1-V reverse bias. The transfer characteristics (I_D versus V_{DS}) for a 1 μm × 250 μm gate all-refractory FET are shown in Fig. 3, and indicate good transistor properties. Figure 4 shows the extrinsic transconductance (g_m) and drain current (I_D) as a function of the gate-to-source voltage (V_{GS}) for the same device at a drain to source voltage (V_{DS}) of 2.5 V. A sharp pinch-off is obtained at V_T = −2.2 V. For $V_{GS} > -2.2$ V the transconductance increases almost linearly with the gate voltage and peaks at 140 mS/mm due to the onset of significant forward gate leakage current at V_{GS} = 0.4 V. Likewise, as expected, the drain current I_D increases with V_{GS} and reaches a value of 232 mA/mm at V_{GS} = 0.8 V as shown in Fig. 4. The drain conductance was measured to be 10 mS/mm at peak g_m. Similar dc characteristics and transconductance values were obtained for the control devices with identical geometries fabricated in conventional FET layer structures without the graded-InGaAs layers and using standard AuGe/Ni/Au ohmic contact metallization.

IV. Summary

We have investigated an all-refractory GaAs FET which uses non-alloyed ohmic contacts consisting of amorphous $TiWSi_x$ refractory metallization and graded-InGaAs layers. Contact resistivities as low as 1×10^{-6} Ω·cm^2 have been obtained and remained stable up to 500° C. The I–V transistor characteristics of the resulting FET's were comparable to those of conventional devices with AuGe/Ni/Au contacts. Maximum peak transconductance values of 140 mS/mm were obtained. These results suggest that state-of-the-art all-refractory FET's with nonalloyed ohmic contacts can be realized for high

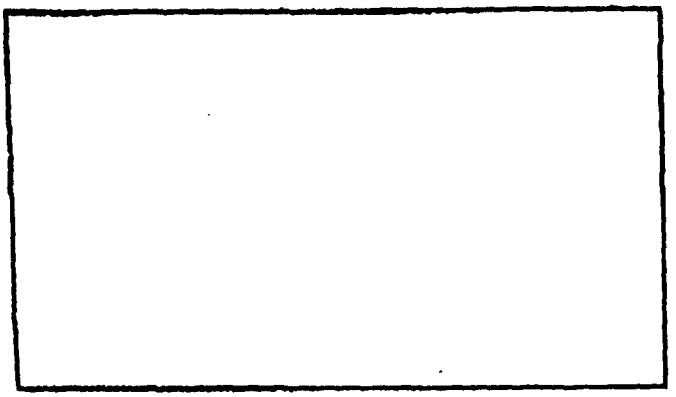

Fig. 3. Transfer characteristics of a typical 1 μm × 250 μm gate all-refractory FET.

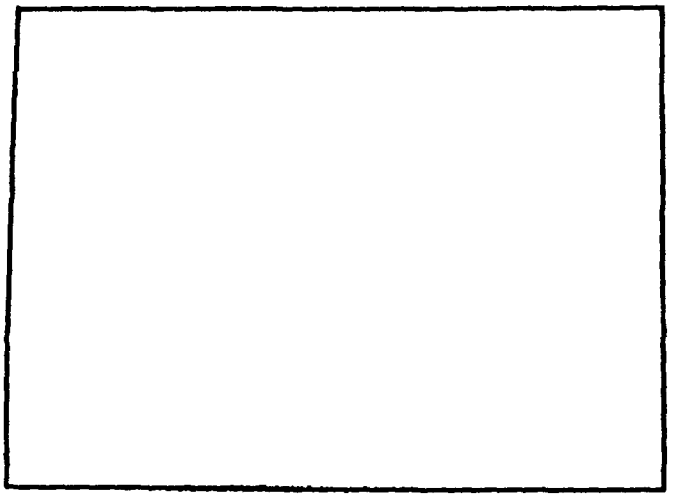

Fig. 4. Extrinsic transconductance (g_m) and drain current (I_D) as a function of gate-source voltage (V_{GS}) for a 1 μm × 250 μm all-refractory FET.

temperature and high reliability discrete and integrated device applications.

ACKNOWLEDGMENT

The authors would like to acknowledge W. Moore and M. F. Zybura for their assistance in the fabrication of the devices.

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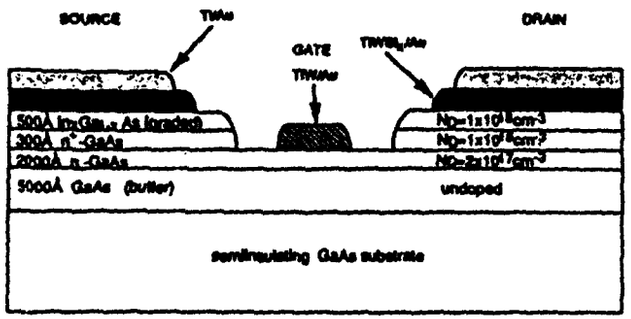
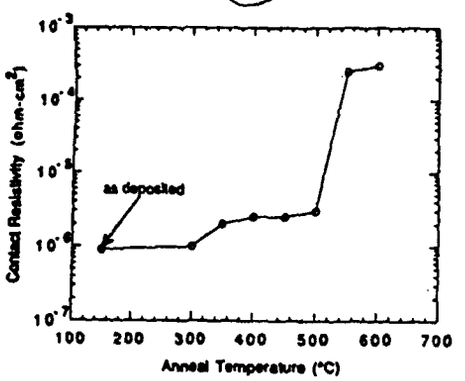


PAPANICOLAOU, JONES, ET AL. EDL-15, no. 1, Jan '94

FIG. 1


Contact Resistivity (ohm-cm²)
as deposited
Anneal Temperature (°C)

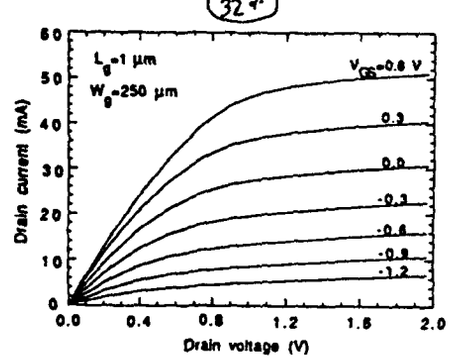

L_g=1 μm
W_g=250 μm
V_GS=0.6 V
0.3
0.0
-0.3
-0.6
-0.9
-1.2
Drain current (mA)
Drain voltage (V)

Fig. 4

P.M. Nicolaou, IEEE S. El Al. EDL-15, No. 1, Jan '94

High Selectivity Patterned Substrate Epitaxy of $In_xGa_{1-x}As/GaAs(0 \leq x \leq 1)$ by Conventional LPOMVPE

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ABSTRACT

A study of $In_xGa_{1-x}As/GaAs$ $(0 \leq x \leq 1)$ selective epitaxy by conventional low-pressure organometallic vapor phase epitaxy (LPOMVPE) was performed using a variety of masking materials. Very low or zero nucleation of polycrystalline (poly) GaAs, $In_{0.7}Ga_{0.3}As$, and InAs was observed on the 300°C chemical vapor deposition (CVD) SiO_2, sputtered SiO_2, and plasma enhanced CVD (PECVD) Si_3N_4 masking materials over a wide range of typical growth parameters. Dense polycrystalline nucleation was observed on TiW masks. The degree of selectivity achieved *vs.* mask material and InGaAs composition at relatively low LPOMVPE reaction temperatures was examined. It was repeatedly observed that during selective epitaxy, zero polycrystalline GaAs and InAs nucleation occurred on the dielectric masks using conventional LPOMVPE. High selectivity in mask areas as large as 500 μm × 500 μm was achieved without specifically using a chloride precurser, or extremely low pressure, or SiN_x masks.

Selective epitaxy of InGaAs/GaAs refers to the growth of epitaxial material in the window openings of a mask that partially covers a GaAs substrate and zero nucleation of material onto the mask itself. The selective growth of semiconductor epitaxial layers has important applications to future electronic and photonic devices and circuits. For example, this technology can be used to fabricate field effect transistors (FETs) with low resistivity, non-alloyed ohmic drain and source contacts. In particular, selectivity deposited InGaAs ohmic contact structures provide reductions in the source resistance,[1] improved short channel effects,[2] and refractory ohmic contacts to n-GaAs.[3] The fabrication of monolithically integrated compound semiconductor circuits also greatly benefits from InGaAs/GaAs patterned substrate epitaxy (PSE) technology; PSE makes it possible to process different material or device structures adjacent to each other within a monolithic circuit. To achieve high quality and high yield integrated circuits (ICs) via PSE requires the further advancement of selective epitaxy technology. As Aboulhouda *et al.* state, "The mastery of growth techniques for heteroepilayers with large lattice mismatch, and the knowledge of a selective epitaxy method to deposit what we want exactly where we want"[4] are the primary obstacles to creating high performance ICs using PSE. It has been shown that PSE can be used to improve the quality of InGaAs/GaAs heteroepitaxial layers.[5,6] In regard to the second criteria, an analysis of the selectivity of GaAs PSE using atmospheric pressure OMVPE was made by Yamaguchi and Okamoto.[7] The authors indicate that limited selectivity can be achieved by an appropriate choice of the mask material, mask geometry, and by raising the growth temperature. Also, it is inferred that low pressure will improve deposition selectivity. In fact, Kamon *et al.* have obtained excellent selectivity using SiN_x masks and a reaction pressure of 10 Torr.[8] They indicate a necessity to use SiN_x as a masking material.

Kuech *et al.*[9,10] and Azoulay *et al.*[11] have stated the need to employ a chloride precurser with the OMVPE growth process to avoid nucleation on the masking material. The chloride molecules competitively cover sites for surface adsorption and destabilize adsorbate reactions which ultimately precludes the surface reaction and attachment of polycrystalline GaAs. Although these modified OMVPE techniques utilizing extremely low pressure or HCl incorporation certainly guarantee zero polycrystalline nucleation, they complicate the mature LPOMVPE process which is now routinely used for complex heteroepitaxy.

We have repeatedly found, and report here, that very little or zero $In_xGa_{1-x}As$ $(0 \leq x \leq 1)$ nucleation will occur on the mask over a wide range of conventional LPOMVPE growth parameters; masked regions up to at least 500 × 500 μm using a variety of different masking materials have been studied. This process has been used to selectively deposit InGaAs non-alloyed ohmic contact structures for FETs without any polycrystalline deposition on the masking material. By employing conventional LPOMVPE, one can avoid the cost of altering the LPOMVPE system, process, and technology already in-place.

Experimental Procedure

Selective epitaxy of GaAs and $In_xGa_{1-x}As$ was performed on (100) Si doped (4×10^{18} cm^{-3}) GaAs substrates with 2° misorientation toward (110). The desired mask (see Table I) was deposited on the substrates and then patterned with a standard positive resist photolithography procedure. These masks include 350°C CVD SiO_2, sputtered SiO_2, PECVD Si_3N_4, and magnetron sputtered TiW. The dielectric mask layers were then selectively etched using BHF or plasma etching to define areas for selective single-crystal epitaxy; a lift-off process was used to define the TiW patterns. All of the mask materials used were approximately 1000 Å thick.

The selective epitaxy study employed two mask geometries. The first mask geometry consisted of 200 × 200 mil square blocks containing long rectangular mask openings or "lines" with widths and separations ranging from 1 to 100 μm. Most of the regions within each block are 100 × 4000 μm. In addition to the blocks containing lines, a large unpatterned area (100 by 200 mil) and small square and triangular windows (1-100 μm^2) are defined in the given mask. The total ratio of mask area to GaAs substrate area on each chip is approximately one to one. The second mask geometry was used to define the 250 × 250 μm drain and source contacts to GaAs FETs. For this geometry, masking regions at least 500 × 500 μm are included. The mask to semiconductor area ratio is about ten.

After creating the pattern, the masked substrates were prepared for crystal growth by LPOMVPE. This pretreatment pro-

Table I. Nucleation densities on unpatterned and patterned masks.

Sample	GaAs nucleation events/10^4 μm^2	InAs nucleation events/10^4 μm^2	Ohmic contact structure events/10^4 μm^2
SiO_2 (350°C, CVD)	3.25 ± 0.25	24 ± 2	52 ± 8
SiO_2 (Sputtered)	925 ± 50	2062 ± 375	521 ± 42
Si_3N_4 (300°C, PECVD)	48 ± 4	20 ± 2	57.5 ± 9
TiW (Magnetron sputtered)	Dense poly	Dense poly	Dense poly
All patterned dielectric masks	0	0	0

cess included a 5 s BHF etch to remove any native oxide from the exposed GaAs and contaminates from the dielectric surface, a 1 min 1:1:50 H_2SO_4:H_2O_2:H_2O etch to remove 600 Å of GaAs, and solvent cleaning using trichloroethylene, acetone, and 2-proponol. Extensive DI rinsing occurred between each etch step. Prior to growth, the samples were cycle purged for 30 min and then *in situ* baked at 675°C for 10 min in a H_2/AsH_3 overpressure (P_{AsH_3} 4.25 · 10 ⁻¹ Torr). Low-pressure vapor phase epitaxy was performed in a horizontal Crystal Specialties LPOMVPE reactor. The reactor temperature was typically between 600 and 675°C. The reactant sources were trimethylgallium (TMG), trimethylindium (TMI), and 10% AsH_3 in H_2. The TMG and TMI bubbler temperatures were 10 and 21°C, respectively. Both bubblers were kept at 760 Torr, while the reactor pressure was maintained at 76 Torr. Palladium purified H_2 was used as the carrier gas for all growth steps. Typical total H_2 flow rates were about 8 l/min. TMG partial pressures between 7.5×10^{-3} Torr and 2.2×10^{-2} Torr and an AsH_3 partial pressure of 4.5×10^{-1} Torr were used. These parameters are typical for the GaAs FET, Gunn diode, and Schottky diode structures, as well as InGaAs non-alloyed ohmic contact structures typically grown with this system. Growth rates were varied from 650 to 1200 Å/min, and growth times between from 15 to 58 min were used.

Three basic structures were grown on both patterned and unpatterned samples to compare nucleation densities. For the majority of experiments, we grew ≈2 μm of either GaAs or InAs, or a 1400 Å graded InGaAs ohmic contact structure. The ohmic contact structure consisted of an 800 Å highly doped n^+ GaAs layer followed by a 600 Å graded $In_xGa_{1-x}As$ layer with increasing indium concentration toward the surface. Other $In_{0.08}Ga_{0.92}As$/GaAs structures were selectively deposited and included in this nucleation study.[6] In each experiment the deposition was compared between unpatterned GaAs, unpatterned 1 × 1 cm dielectrics or TiW, and various patterned substrates (Table I). Analysis was completed using a scanning electron microscope, an optical microscope, an ellipsometer, and a probe station.

Results

The dielectric constants of the deposited masks were ϵ_r = 2.15 for the 350°C CVD SiO_2, ϵ_r = 2.13 for the sputtered SiO_2, and ϵ_r = 4.22 for 300°C PECVD Si_3N_4 as determined by ellipsometry. To ensure resultant nucleation was not an advent of pinholes, etch tests, lift off, and current continuity checks were performed. We concluded there to be negligible pinhole resultant nucleation. Figure 1 shows a SEM micrograph of InAs nucleation on an unpatterned 1 × 1 cm film of SiO_2 on a GaAs substrate. In Fig. 2, the companion InAs epitaxy on a patterned SiO_2/GaAs substrate is shown. The line and masked regions shown in the photos are 100 μm in width and 4000 μm in length. Figure 3 is a photomicrograph of FET source/drain regions with a selectively grown non-alloyed ohmic contact structure used for FET fabrication. The drain to source spacing of the top FET patterns is about 5 μm. This figure demonstrates approximately 500 × 500 μm of nucleation free mask

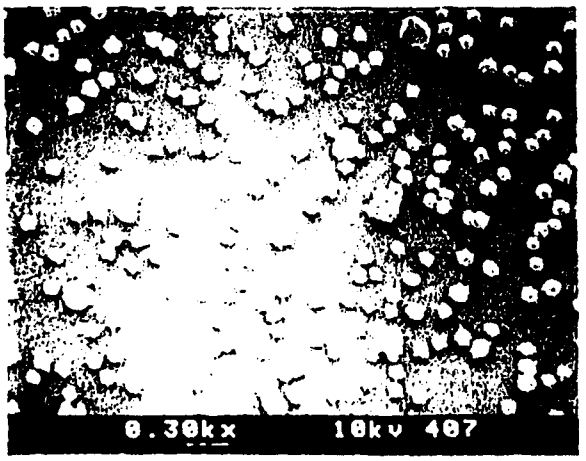

Fig. 1. Top view of an unpatterned SiO_2/GaAs substrate after 50 min of InAs LPOMCVD. A companion unpatterned GaAs substrate exhibited 2 μm of epitaxy. Very little nucleation is observed for $In_xGa_{1-x}As$ ($0 \leq x \leq 1$). (T = 600°C).

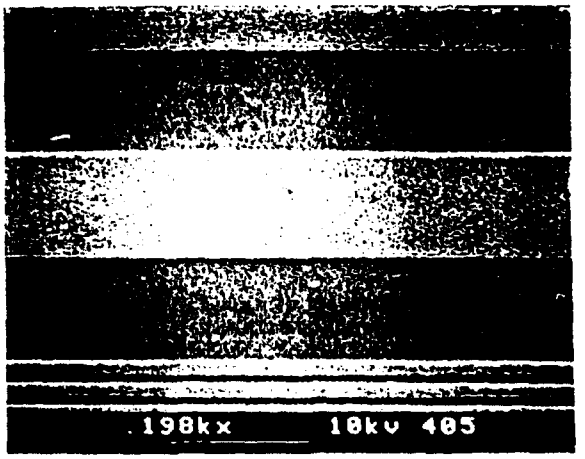

Fig. 2. Top view of a patterned SiO_2/GaAs substrate after 2 μm of InAs growth in the windows and zero nucleation on the mask. (T = 600°C).

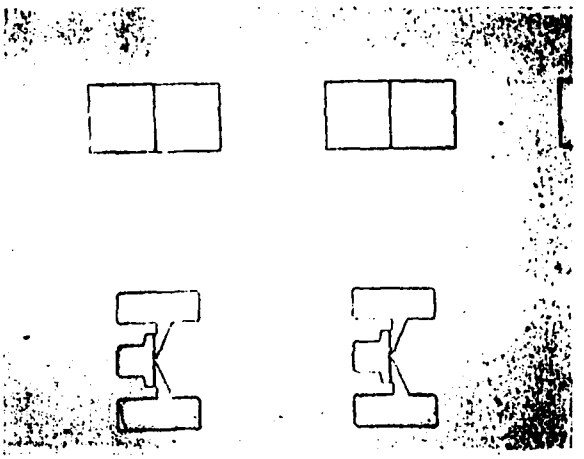

Fig. 3. Top view of an InGaAs ohmic contact structure selectively grown in FET drain/source windows. Zero $In_xGa_{1-x}As$ ($0 \leq x \leq 1$) nucleation is observed on the Si_3N_4 mask. (T = 600°C).

area. In all cases there is very little $In_xGa_{1-x}As$ ($0 \leq x \leq 1$) nucleation on the dielectric substrate, and for the patterned substrates, zero nucleation on large masked regions was observed. These results are typical for the many $In_xGa_{1-x}As$ ($0 \leq x \leq 1$) growth performed using the dielectric masks, and the full range of growth parameters metntioned.

Table I shows the corresponding nucleation densities for the three material structures, and the four unpatterned masks employed. The densities were obtained by choosing several typical regions on the mask surface of equal area and counting the nucleation occurrences (polygrains). The error associated with each value is the greatest difference in nucleation count between any two such areas. Thicker selective epitaxial layers than shown in Table I have also demonstrated high selectivity. In several instances ≈10 μm of GaAs was grown on SiO_2 patterned GaAs samples with no observed nucleation on the masked areas. Unlike the dielectric masks, the TiW masked samples were dominated by polycrystalline nucleation.

The differences in surface nucleation processes between high quality CVD SiO_2 and CVD Si_3N_4 masks appear to be technologically inconsequential when grown at low pressure. The zero mask nucleation on the dielectrics is attributed to smooth, dense, and pinhole free dielectric films, a thorough cleaning procedure, a substrate pre-bake to reduce nucleation centers, and a large P_{AsH_3}/P_{TMG} ratio resulting in high, competitive AsH_3 mask coverage and a limited coverage of Ga constituents on the mask. When masking materials with rougher surfaces were used, *i.e.*, TiW and sputtered SiO_2, the nucleation events increased significantly. This would agree with the research done by Yamaguchi and Okamoto,[7] where they cite increased nucleation on rough surfaces.

Conclusion

Using a conventional LPOMVPE system with a variety of masking materials, high selectivity patterned substrate epitaxy was achieved when growing $In_xGa_{1-x}As/GaAs$ ($0 \leq x \leq 1$) structures. Zero mask nucleation events were repeatedly observed in areas at least as large as 500 × 500 μm (see Fig. 3). Our high selectivity results are obtained without a chloride precurser, and by using low to moderate growth temperatures, at typical low pressures. Improved selectivity is primarily associated with the high quality of the dielectrics, smooth mask surfaces, and a H_2/AsH_3 prebake prior to growth.

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Effect of Electrochemical Treatments on the Photoluminescence from Porous Silicon

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ABSTRACT

In order to understand the mechanisms which limit the quantum efficiency of visible light emission from porous Si, the effects of electrochemical treatments on the luminescence intensity as well as the spectra have been studied in aqueous solutions. A strong improvement of the luminescence intensity has been noted in each step of the following sequential treatments in acid solution (0.1*N* H_2SO_4): (*i*) immersion into the electrolyte; (*ii*) anodic polarization; and (*iii*) desiccation. The only degradation of intensity has been observed in neutral solution (0.1*M* Na_2SO_4) following similar electrochemical treatments, although some recovery of the intensity has been noticed during anodic polarization. These photoelectronic behaviors, combined with our independent TEM observation of the porous Si, strongly suggest that the porous layer has a heterogeneous structure composed of a photo-absorptive, amorphous Si-like medium and Si clusters, dispersed in the medium, which act as emission centers.

The recent discovery of visible light emission from porous silicon[1] has stimulated both experimental and theoretical investigations in the application of Si as an optoelectronic device material. In order to understand the emission mechanism, we have been doing a systematic study to control the numerous parameters which may affect the luminescence intensity, as well as the peak photon energy. In the present study, we will show that the PL intensity and the peak photon energy of the spectra are strongly affected by electrochemical treatments in aqueous solutions. In relation to the present work, Halimaoui *et al.*[2] have reported the observation of electroluminescence in the visible range during anodic oxidation of porous Si in aqueous electrolytes.

Porous Si layers were prepared on Si pellets (10 × 10 mm) cut from p-type wafers [(100), 1-2 Ω · cm)] using various anodization procedures. In order to make an electrical contact on each sample, platinum was sputter-deposited on the back surface and then heat-treated at 600°C for 20 min. After a copper wire was connected to the Pt surface using Ag paste, the entire sample, except for the front surface, was coated with epoxy resin. The samples used in the present study were prepared by galvanostatic anodization at 1 mA/cm² for 60 min in 48% hydrofluoric acid at room temperature. The porous layer formation was performed under room-light (light intensity ~10 μW/cm²). The formation rate of the porous layer, determined from SEM photos, was 2.2×10^{-4} cm³/C under the above anodization conditions. The emission color was checked using a 6 W handy mercury lamp (λ = 365 nm). The luminescence spectra were measured using an argon-ion laser excitation (488 nm, 20 mW) combined with a monochromator and a Si (or a cooled Ge) photodiode. A computerized lock-in detection system was established for the present experiment. In order to make electrochemical measurements, the sample was placed in an electrochemical cell where the counterelectrode (Pt) and a saturated calomel reference electrode (SCE) were immersed in the same electrolyte, either 0.1*M* Na_2SO_4 or 0.1*N* H_2SO_4. We chose these electrolytes (neutral and acid solutions) with the same anions (SO_4^{2-}), because, in our independent electrochemical study on porous titania,[3] we noticed that the anodic current at a constant potential depends upon the ionic radii of anions in the electrolytes.

A typical PL spectrum from porous Si measured in air is shown in Fig. 1. We noticed that there are at least three independent emission peaks in the spectrum: The first is a broad peak in the energy range between 0.9 and 0.8 eV, while the second is a shoulder that appeared in the energy range between 1.1 and 1.2 eV. The third is the visible light emission that peaked in the energy range between 1.6 and 1.9 eV which depended upon the preparation conditions. The intensities of the peaks are several orders of magnitude stronger than that of the bandgap emission from single-crystalline Si. Compared with the PL spectra obtained from Si fine particles prepared by gas-evaporation technique,[4] the first peak at about 0.8 eV was assigned to the emission associated with the Si dangling-bonds within the porous layer. The energy range of the second peak coincides with the bandgap energy of crystalline Si

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A Simplified Model Describing Enhanced Growth Rates During Vapor Phase Selective Epitaxy

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Abstract

Nonuniform and enhanced growth rates are calculated for vapor phase selective epitaxy. By solving Laplace's equation above a partially masked growth substrate the effects of gas phase diffusion on vapor phase selective epitaxy are considered. Surface features having a single dielectric masking stripe or a series of periodically spaced masking stripes are analyzed. Closed form expressions are given for reactant concentrations and enhanced growth rates away from the edge of a large single masking stripe, and similar numerical calculations are made for the case of repetitive masking stripes. These calculations compare favorably with Low Pressure Organometallic Vapor Phase Selective Epitaxy of GaAs and InAs on SiO_2 masked GaAs substrates.

1 Introduction

Selective epitaxy is an important circuit fabrication technology that allows dissimilar heterostructure materials to be deposited adjacent to one another within a monolithic circuit[1]. However, the presence of the dielectric masking material on the substrate severely alters growth rates, and makes it difficult to control growth rates across the sample. In particular, the growth rate is nonuniform and enhanced away from the edges of large regions of dielectric mask. Furthermore, these enhancements vary with the mask geometry. In order to use selective epitaxy for integrated circuit fabrication, some estimation of enhanced growth rates as a function of mask geometry is needed.

In this paper, a simplified mathematical model is presented that describes the effects of gas phase diffusion on enhanced growth rates during selective epitaxy in a horizontal Low Pressure Organometallic Vapor Phase Epitaxy (LPOMVPE) reactor. Calculations of the reactant concentration, the concentration flux, and the growth flux at the surface during selective epitaxy are completed by solving Laplace's equation above a masked substrate. Other models have been developed to describe nonuniform and faceted growth at the substrate/mask interface during selective

epitaxy[2], and at the edge of an etched trough during non-planar substrate epitaxy[3, 4]. However, the analytical model described here is specifically meant to predict nonuniform and enhanced growth rates far from the substrate/mask interface. Also, solutions to Laplace's equation for a single etch trough during patterned substrate epitaxy, which is substantially different than selective epitaxy, have been made numerically by C.H.J. van den Brekel[5].

Using a relatively simple conformal mapping technique, we offer analytical expressions that can be used to estimate enhanced growth rates as a function of the masking geometry. The primary result of this research is a mathematical estimation of nonuniform and enhanced growth rates during vapor phase epitaxy of semiconductors on dielectric patterned semiconductor substrates. The solution to the problem shown in Figure 1 characterizes the effects of long range gas phase diffusion; and the solution to the problem shown in Figure 3 describes the relationship between enhanced growth rates and mask window geometries. Such estimations are needed to reliably use selective epitaxy for compound semiconductor integrated circuit fabrication.

2 Model for a Single Masking Stripe

In Figure 1a, C is the reactant concentration, C_o is the reactant concentration at the top of an effective boundary layer of height δ^*, and $\frac{\partial C}{\partial n}$ is the concentration gradient normal to the surface. The analytical results of Van de Ven *et al.*[6] and numerical results of Jansen *et al.*[7], show the reactant concentration above the substrate up to δ^* is considered to be controlled predominately by molecular diffusion. Therefore, for unmasked substrates, the concentration varies nearly linearly between the surface and δ^*. This idealization is justifiable for the case of GaAs and $In_xGa_{1-x}As$ organometallic vapor phase selective epitaxy since the observed non-uniform enhanced growth rates are not a strong function of the gas flow direction, or the surface morphology. Using equation 4 in reference 6, δ^* can be estimated as a function of reactor geometry and gas flow velocity.

In order to analytically solve the boundary value problem over a semiconductor substrate that has a single dielectric mask stripe, as shown in Figure 1a, without using numerical methods, we must transform the domain. The aim of the transformation is to place the discontinuities in the boundary conditions along the substrate to the corners in the new domain. Figure 1a illustrates the initial cell geometry and the boundary conditions.

Since the mask region straddles the origin, we need to consider only half the cell if the boundary condition $\frac{\partial C}{\partial y}\mid_{y=0}= 0$ is used. We assume that no growth occurs along the masked area so that the normal flux of the growth constituents at the mask surface is zero ($\frac{\partial C}{\partial x}\mid_{x=\delta^*/2}= 0, y \leq \ell/2$). Similarly, the semiconductor surface reaction rates are considered to be infinitely fast, and the reactant concentration is set to zero at the semiconductor growth surface ($C|_{x=\delta^*/2}= 0, y \geq \ell/2$). At $-\delta^*/2$, the top of the effective boundary layer, the concentration is constant ($C|_{x=-\delta^*/2}=C_o$).

For the single mask stripe, the required Schwarz-Christoffel transformation reduces to the sine function. First, the dimensionless coordinates $x_1 = \pi x_I/\delta^*$, $y_1 = \pi y_I/\delta^*$ are introduced with $z_1 = x_1 + iy_1$. The sine transformation followed by a scaling and an inverse sine transformation create a domain where C can be identified by inspection (Figure 1e),

$$C = -\frac{C_o}{\pi}x_4 + \frac{C_o}{2}. \tag{1}$$

The constant concentration profiles in the initial cell (Figure 1a) can be obtained from (1) by the chain of substitutions,

$$x_4 = \Re e z_4, \tag{2}$$

$$z_4 = \sin^{-1} z_3, \tag{3}$$

$$z_3 = \frac{2z_2 + 1 - \cosh a}{1 + \cosh a}, \tag{4}$$

$$z_2 = \sin z_1, \tag{5}$$

and

$$z_1 = \pi z_I / \delta^*. \tag{6}$$

After completing all the above substitutions into (1),

$$C = -\frac{C_o}{\pi} \Re e \left[\sin^{-1} \left(\frac{2 \sin z_I + 1 - \cosh a}{1 + \cosh a} \right) \right] + \frac{C_o}{2}, \tag{7}$$

where $a = \ell/2$ and $z_I = \frac{\pi}{\delta^*}(x + \imath y)$. Equation 7 can be used to calculate the reactant concentration during selective epitaxy above a single dielectric masking stripe on a semiconductor surface. The normal and tangential fluxes are written in terms of the partial derivatives

$$\frac{\partial C(x,y)}{\partial x} = -\frac{C_o}{\pi} \Re e \left(\frac{\cos z_I}{([\cosh(\frac{\pi \ell}{2\delta^*}) - \sin z_I][\sin(z_I) + 1])^{1/2}} \right) \tag{8}$$

$$\frac{\partial C(x,y)}{\partial y} = -\frac{C_o}{\pi} \Re e \left(\frac{\imath \cos z_I}{([\cosh(\frac{\pi \ell}{2\delta^*}) - \sin z_I][\sin(z_I) + 1])^{1/2}} \right). \tag{9}$$

The components of the reactant flux normal or parallel to the surface are calculated using equations 8 and 9, respectively. Since the growth rate is equal to the normal component of the reactant flux at the surface, the nonuniform growth rate along the surface and away from the mask is obtained when equation 8 is evaluated at $x = 0$. This is shown in Figure 2 with the mask length, $\ell = 2500\mu$m and $\delta^* = 1.5$cm.

3 Model for a Periodic Masking Structure

Many selective epitaxy applications involve periodic mask structures where there are sequences of growth regions spaced by dielectric masking regions. The geometry used to calculate the enhanced growth rate for such a structure is shown in Figure 4a, where the boundary conditions are the same as those described for the single dielectric problem of Figure 1.

An overview of the transformations is given in Figure 3. The first step in the solution is to find the appropriate transformation from the z_2 plane of Figure 3c to the z_1 plane in Figure 3b. The Schwarz-Christoffel transformation that accomplishes this is

$$z = f(\zeta) = a \int_0^{\zeta} \frac{d\zeta}{\sqrt{(\zeta^2 - 1)(\zeta^2 - 1/k^2)}}. \tag{10}$$

The location $\frac{1}{k}$ of point D has been determined by iteration using *Mathematica*[8]. After k is determined, The point A can be calculated using the Jacobian elliptic function, $sn(u)$. As illustrated in Figure 3c, the final cell is constructed with discontinuous boundary conditions only at the corners. This is accomplished by scaling, and another Schwarz-Christoffel transformation of the form of equation 10.

The solution to the boundary value problem in this final cell (Figure 3e)

is

$$C = C_o y_4. \tag{11}$$

To calculate the resultant concentration in the initial cell, a given coordinate, (x_4, y_4), of the final cell is mapped back to (x_I, y_I) in the initial cell. The concentration value is assigned to that point with equation 11. Mapping successive points from the final cell to the initial cell requires the use of both the Jacobian elliptic function and the elliptic integral, respectively. Since the solution to these functions is involved, the program *Mathematica* is used to perform the transformations and determine the concentration in the initial cell. The flux terms $\frac{\partial C}{\partial x}$ and $\frac{\partial C}{\partial y}$ are computed numerically, and the value for the flux is normalized such that the difference in concentration between two points a distance δ^* apart is C_0 (the normal component of the reactant flux at the surface is equal to one). Figure 4 shows the reactant concentration along and above the periodically masked surface. The bow in concentration near the substrate-to-mask interface shows the influence of the masking stripe on the gas phase diffusion. Only one period of the masked surface is shown. For this figure $\delta^* = 1.5$cm, and both the growth and mask surfaces are 1500μm wide. The concentration has been calculated using *Mathematica*, and the mapping described above and in Figure 3.

4 Results and Discussion

LPOMVPE selective epitaxy experiments were conducted to compare the theoretical results to experiment. Selective epitaxy of GaAs and InAs was performed on SiO_2 patterned (100) n^+ GaAs substrates with 2^o misorientation toward $< 110 >$. Details of the wafer processing and growth can be found elsewhere [9]. The enhanced growth study used two masking geometries. The first mask geometry corresponds to the single dielectric mask problem. The iterative mask structure (similar to Figure 3a) is mimicked in a different region on the same mask. This mask geometry consists of dielectric regions 4000μm in length, 100μm in width, and 100μm in spacing. Based on the results of Van de Ven *et al.*[6], we have estimated $\delta^* = 1.5$cm for our reactor. Two basic structures were grown on both patterned and unpatterned samples to compare subsequent growth rates. For the majority of experiments, we grew $\approx 2\mu$m of either GaAs or InAs. Analysis of the enhancement was completed using a Tencor surface profiler, which has an associated error of less than 100$\mathring{A}$, and optical and scanning electron microscopy.

The single dielectric mask experimental data, and the associated theoretical calculation using equation 8 with x=0, are shown in Figure 5.

For a 2500μm masked stripe in a large unmasked region, the model predicts that non-uniform, and enhanced growth rates will occur up to approximately 1500μm from the mask edge, and that this phenomena is predominately related to gas phase diffusion. Enhanced growth rates near the mask/semiconductor interface are primarily controlled by surface diffusion and crystallographic effects[2, 3, 4] and therefore are not described by this model. For a given mask width (ℓ) relative to the effective boundary layer thickness (δ^*) in equation 8, one can estimate the distance from the mask over which the growth is nonuniform. Hence, for large growth windows and long masking stripes, equation 8 can be used to predict the extent of growth rate nonuniformity expected when using selective epitaxy.

Also shown in Figure 5 is the calculated growth enhancement for a periodically masked surface. In this case, the growth region is $10,000\mu$m wide, while the masked region is 2500μm wide. Since the growth region is very large relative to the mask region, very little enhancement is observed beyond 1500μm from the mask edge. This figure shows that as the growth region becomes very large, the solutions of both cases converge as expected. When the masking regions are sufficiently close, significant growth rate enhancement in the substrate regions will be observed. As described above, *Mathematica* is used to solve the general periodic mask problem outlined in

Figure 3. From these calculations one can predict the extent of growth rate enhancement as a function of mask geometry by again varying the mask length, and the mask spacing relative to the effective boundary layer thickness. Figure 6 shows the enhanced growth rate for small periodic masking structures. The mask width is kept constant at 100μm and the growth region is 10μm or 100μm with $\delta^* = 1.5$cm. Included in this figure are experimental data from both GaAs and InAs LPOMVPE experiments with the mask length and spacing equal to 100μm. For the case of $\delta^* = 1.5$cm, and $\ell = 100\mu$m, there is essentially no enhancement in the center of the growth region for mask spacings greater than 1000μm (not shown). As the spacing is reduced, the enhancement increases. When the semiconductor growth surface and dielectric mask widths are both 100μm, the growth rate is enhanced by a factor of two around the mask interface, and by approximately a factor of 1.6 near the center of the growth region. As the growth region is further reduced to 10μm, the overall nonuniformity is not as large, but the enhancement is dramatically increased to a factor of seven.

The theoretical solution only considers molecular diffusion within δ^* and therefore the solution will not vary with the direction of the gas flow or with the morphology of the growth material. Therefore, experiments were performed using two patterned substrates, one with the mask stripe along the

gas flow direction and the other perpendicular to it, and the variation in enhanced growth between the samples was undetectable. In another experiment GaAs with very poor surface morphology was deposited, and again the enhanced growth rate results were typical. Therefore, the initial premise that forced flow and surface effects be excluded, and that $\nabla^2 C = 0$, is an appropriate approximation provided the boundary conditions at the surface represent the experimental situation. If the surface reaction rate on the semiconductor is not fast relative to the gas phase diffusion rates, or if significant polycrystalline material is deposited on the mask, the boundary conditions are violated, and the accuracy of the model is compromised.

5 Conclusion

In summary, we offer a method for predicting enhanced growth rates during vapor phase selective epitaxy. A closed form solution for the concentration and associated fluxes is derived for the single dielectric mask bounded by infinite growth regions, and to a periodic mask structure through the use of *Mathematica*. Although the model is based on simple constraints, the results concur with experimental data for GaAs and InAs Low Pressure Organometallic Vapor Phase Selective Epitaxy. The derived equations,

mathematical formulations, and experimental results are guidelines for designing selective epitaxy processes and mask geometries for integrated circuit fabrication.

6 Acknowledgements

The authors would like to thank both Wallace Anderson and Nicholas Papanicolaou of the Naval Research Laboratory for their technical support. This work was partially funded by NSF grant # MSS 9008973, and the Naval Research Laboratory, Microwave Branch.

Figure Captions

Figure 1: Sequence of transformations and scalings for the single masking stripe and infinite growth region problem.

Figure 2: Normalized vertical flux profiles for the single masking stripe and infinite growth regions with $\delta^* = 1.5$cm, and $\ell = 2500\mu$m. The mask/growth region interface is at 550μm.

Figure 3: Sequence of transformations and scalings for the periodically masked surface problem.

Figure 4: Reactant concentration profiles calculated using the periodic masking structure solution with both the width of the mask, ℓ, and growth surface equal to 1500μm. ($\delta^* = 1.5$cm, $C|_{\delta^*}=C_o$).

Figure 5: The theoretical solution for the normalized enhanced growth rates using equation 8, with x=0, is given by the solid line. The corresponding solution for a periodically masked surface is given by the dotted line with a growth region of $10,000\mu$m. The associated GaAs experimental data for normalized enhanced growth due to a single mask stripe is also shown. In all cases the mask width, $\ell = 2500\mu$m, and the effective boundary layer, $\delta^* = 1.5$cm.

Figure 6: The calculated normalized growth for a constant mask length of 100μm with 100μm or 10μm growth regions is shown. Experimental data for a 100μm mask/100μm growth region is shown for InAs and GaAs LPOMVPE. ($\delta^* = 1.5$cm)

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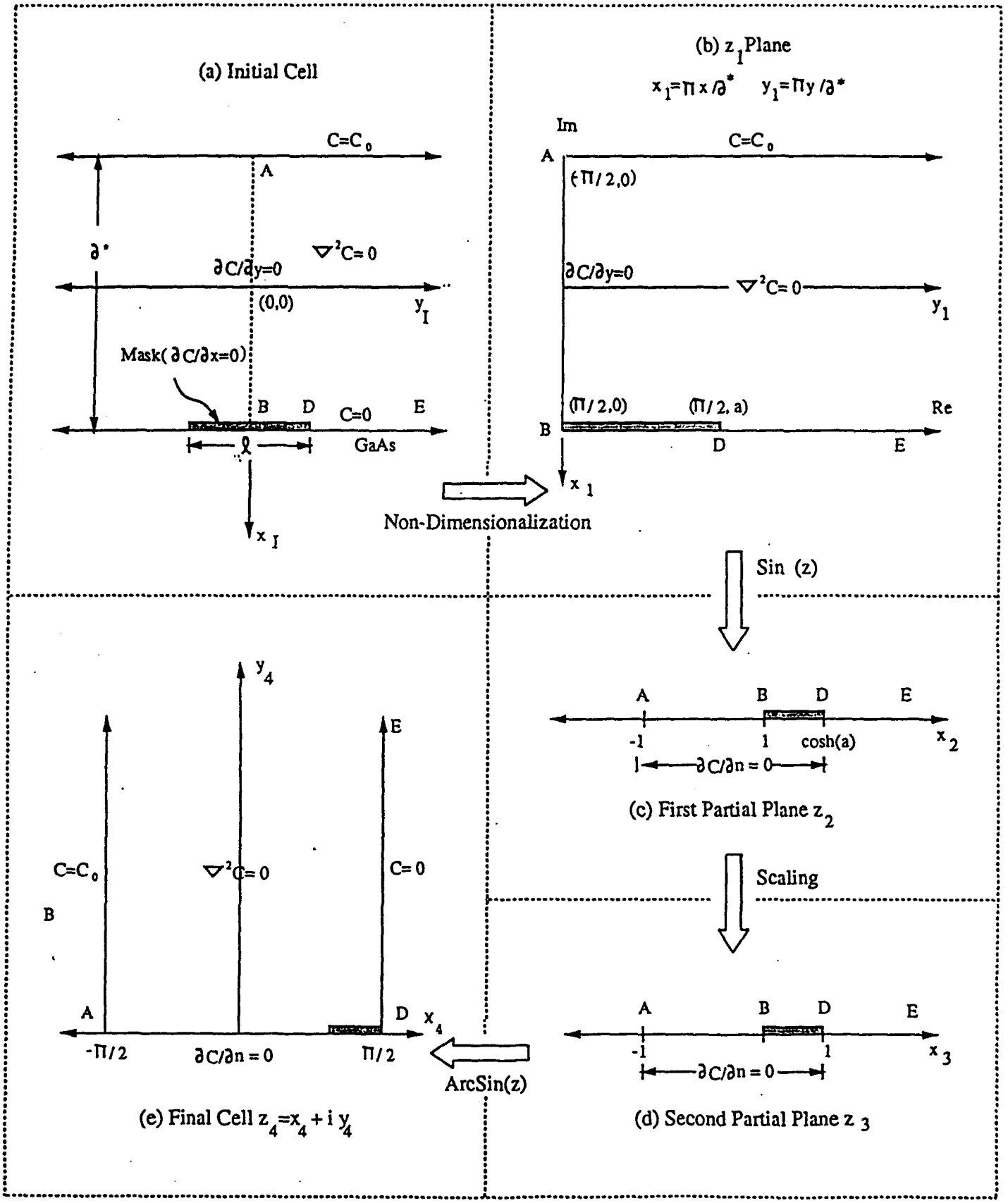
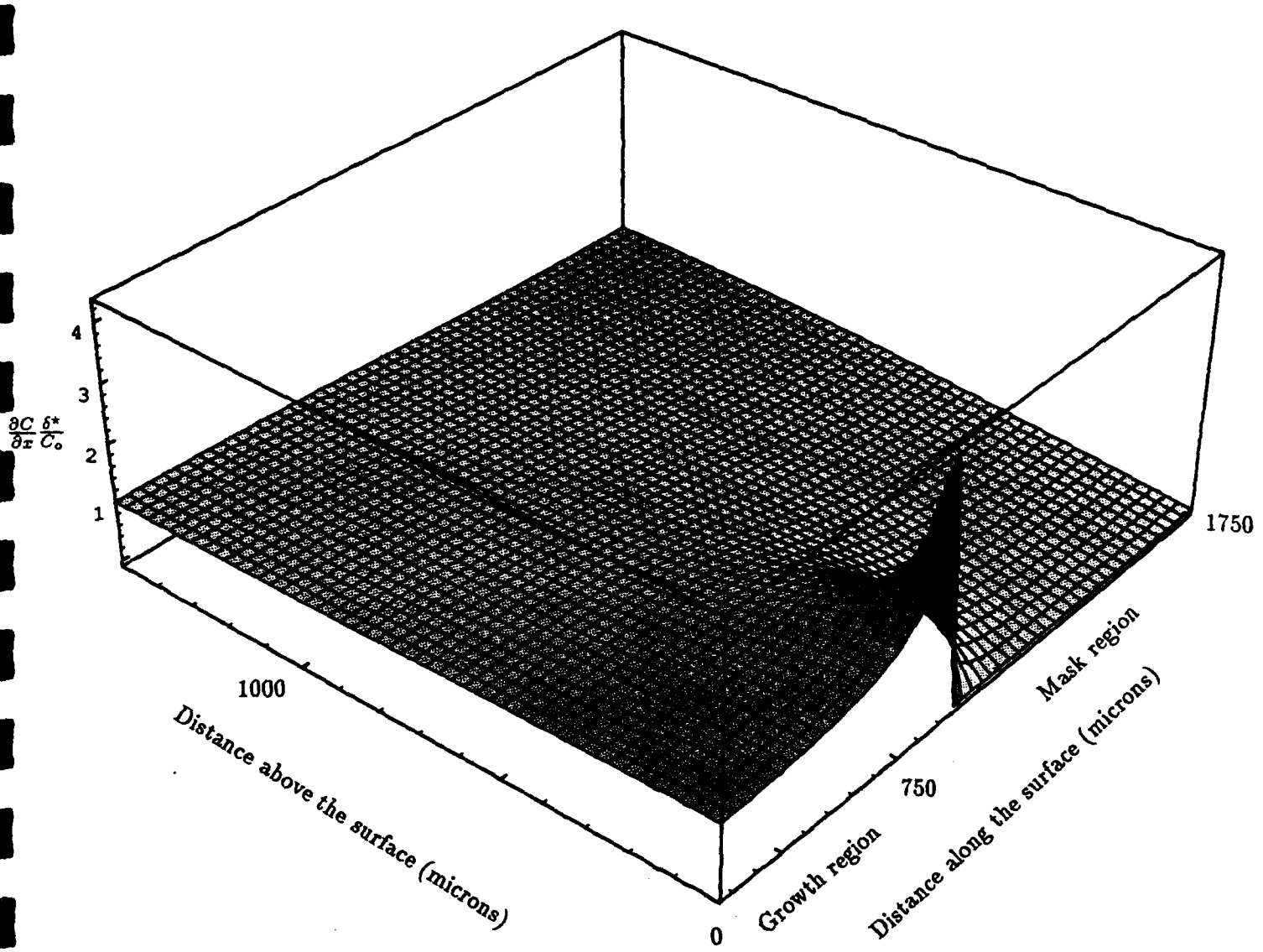
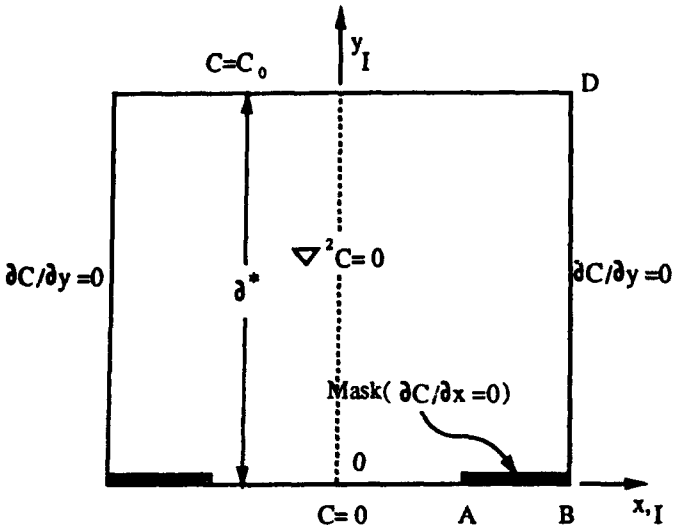
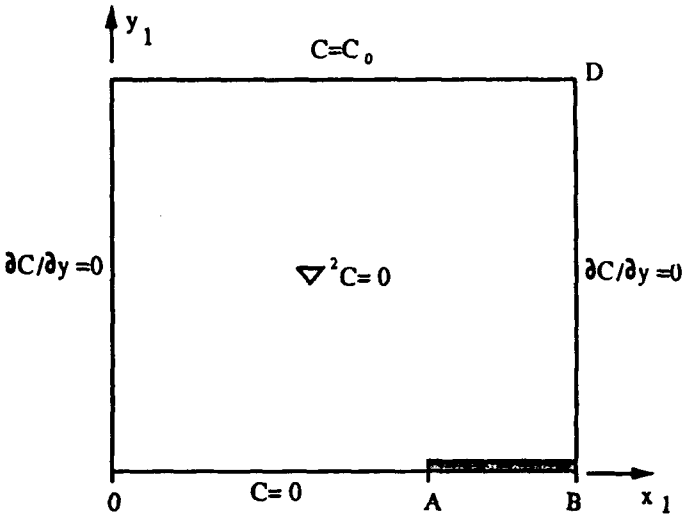

(a) Initial Cell
C=C0
A
∂*
∇²C=0
∂C/∂y=0
(0,0)
yI
Mask(∂C/∂x=0)
B
D
C=0
E
ℓ
GaAs
xI
(b) z1 Plane
x1=π x /∂*
y1=π y /∂*
Im
C=C0
A
(π/2,0)
∂C/∂y=0
∇²C=0
y1
(π/2,0)
(π/2, a)
Re
B
D
E
x1
Non-Dimensionalization
Sin (z)
A
B
D
E
-1
1
cosh(a)
x2
∂C/∂n = 0
(c) First Partial Plane z2
Scaling
A
B
D
E
-1
1
x3
∂C/∂n = 0
(d) Second Partial Plane z3
ArcSin(z)
y4
E
C=C0
∇²C=0
C=0
B
A
D
x4
-π/2
∂C/∂n = 0
π/2
(e) Final Cell z4=x4 + i y4

Figure 1


$\frac{\partial C}{\partial x}\frac{\delta^*}{C_o}$
4
3
2
1
1000
Distance above the surface (microns)
0
750
Growth region
1750
Mask region
Distance along the surface (microns)



(a) Initial Cell

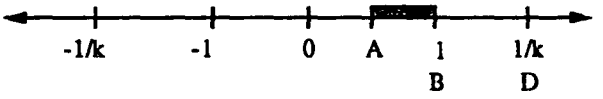


(b) Non-Dimensionalized z 1 Plane

Symmetry Reduction

Elliptic Function

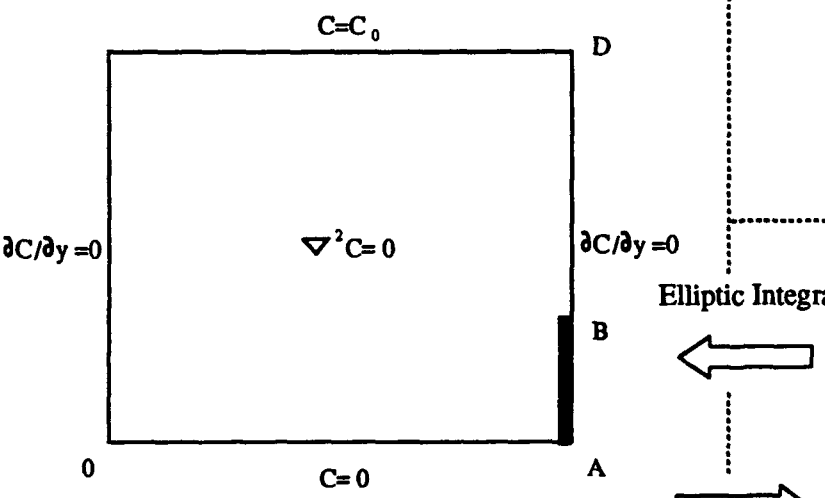
Elliptic Integral



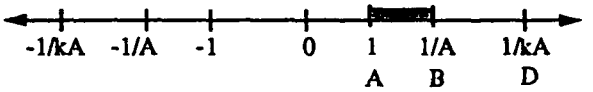
(c) z_2 Plane

1/A ... Scaling ... A

Elliptic Integral



(e) z_4 Plane



(d) z_3 Plane

Elliptic Function

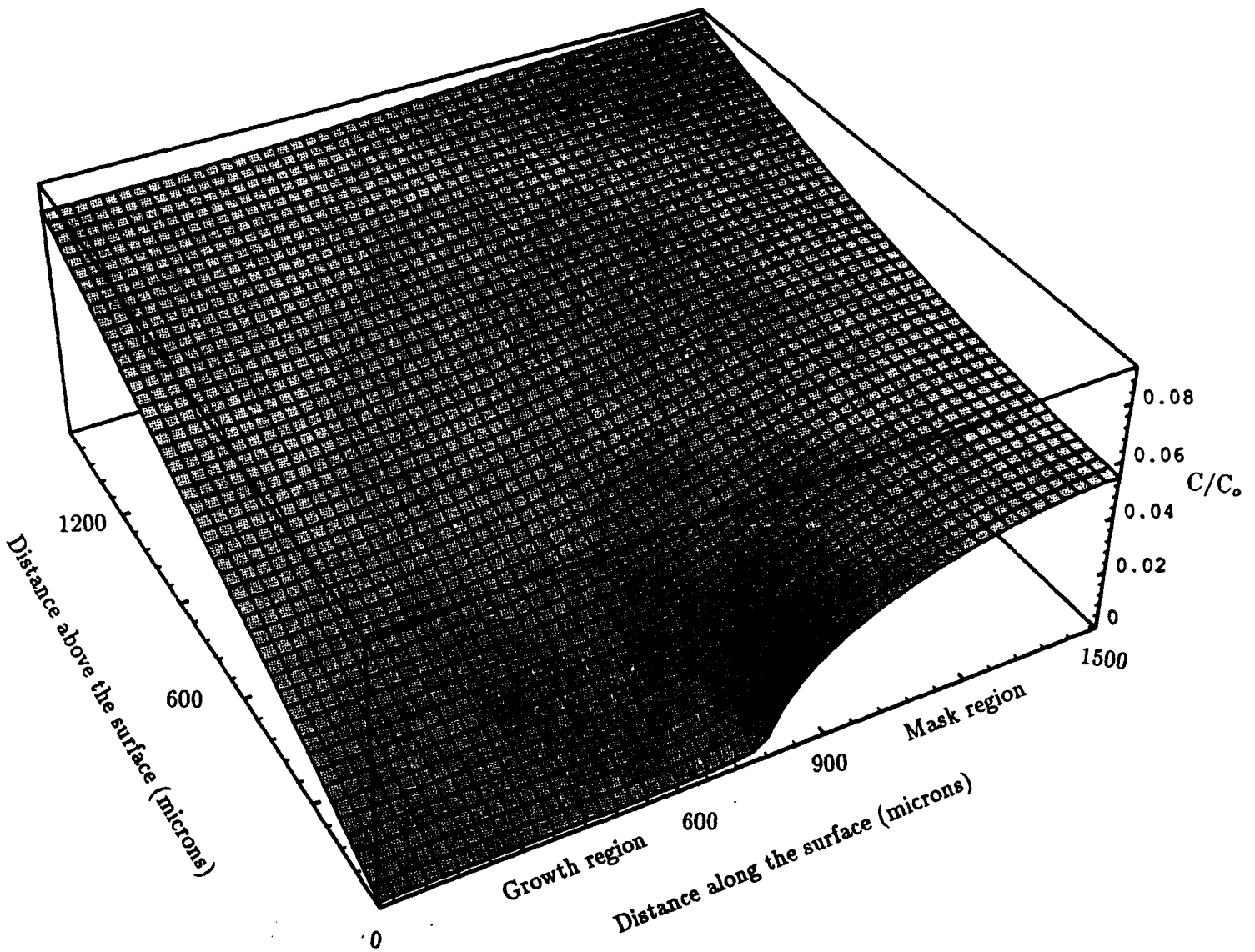

0.08
0.06
C/C₀
0.04
0.02
0
1200
600
0
Distance above the surface (microns)
Growth region
600
900
1500
Mask region
Distance along the surface (microns)

Figure 4

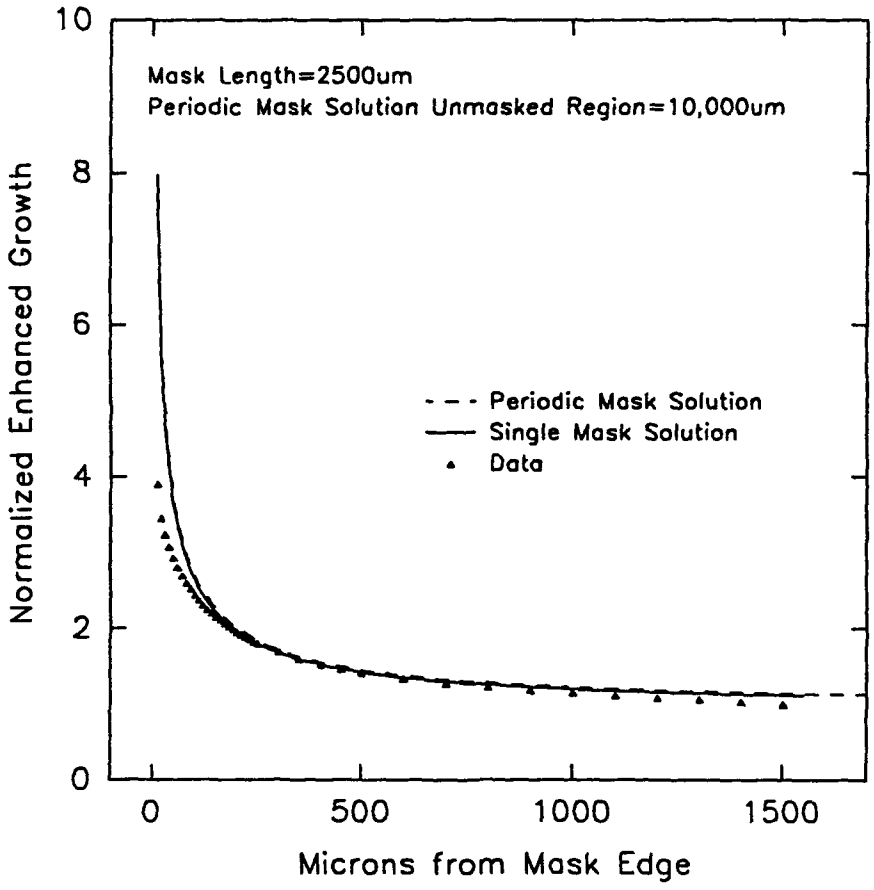

Mask Length=2500um
Periodic Mask Solution Unmasked Region=10,000um
Normalized Enhanced Growth
Microns from Mask Edge
Periodic Mask Solution
Single Mask Solution
Data
0
2
4
6
8
10
0
500
1000
1500

Figure 5

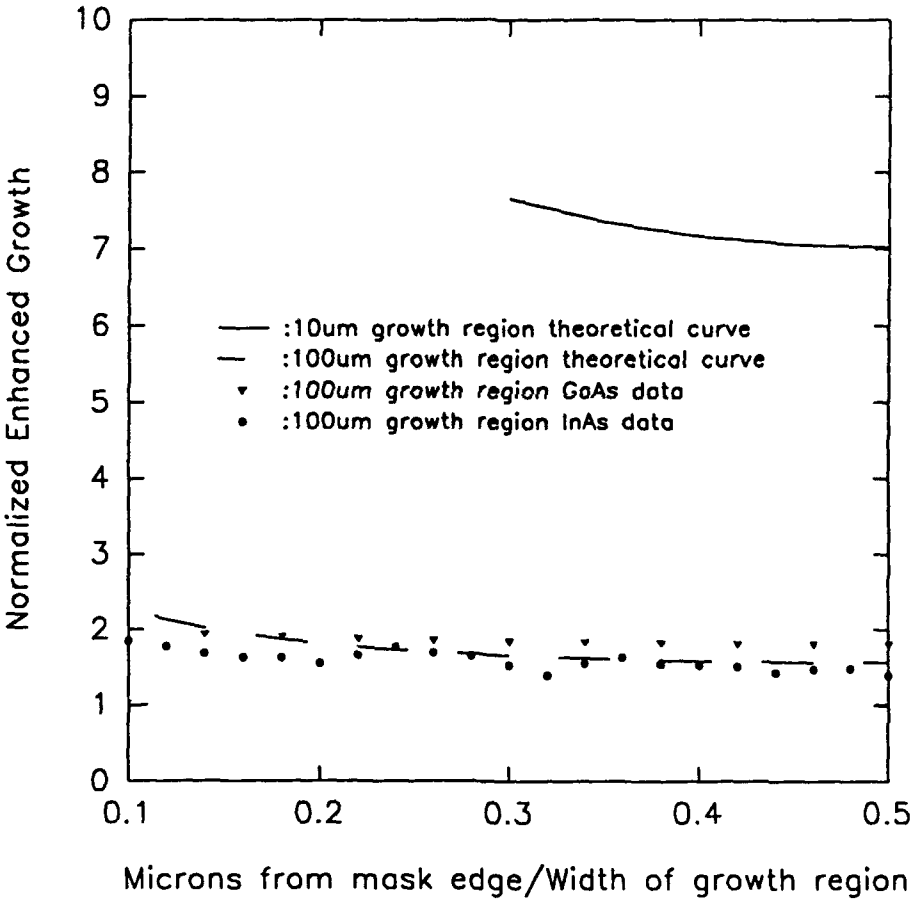

10
9
8
7
6
5
4
3
2
1
0
0.1
0.2
0.3
0.4
0.5
Normalized Enhanced Growth
:10um growth region theoretical curve
:100um growth region theoretical curve
:100um growth region GaAs data
:100um growth region InAs data
Microns from mask edge/Width of growth region

Figure 6

Submitted to The Second International High Temperature Electronics Conference

All-refractory GaAs FET for High Temperature Applications

N. A. Papanicolaou+, S. H. Jones*, J. R. Jones*, and W. T. Anderson+.,

Abstract

This work reports on the investigation of an all-refractory 1 μm-gate GaAs field-effect transistor for high temperature applications. This device employs non-alloyed source and drain ohmic contacts consisting of amorphous (α) $TiWSi_X$ metallization and intervening graded-InGaAs layers grown by Low Pressure Organometallic Vapor Phase Epitaxy (LPOMVPE). The $TiWSi_X$ is formed by alternating layers of TiW(10Å) and Si(1.5Å) sequentially deposited to a total thickness of 500 Å by RF magnetron sputtering. The Schottky gate consists of e-beam deposited TiW/Au (500Å/2000Å) refractory metallization system. The epitaxial layered structure consists of a 0.5mμ undoped GaAs buffer layer, a 2000Å n^+ GaAs active layer doped at $2x10^{17}$ cm^{-3} and 500Å of n^+ GaAs followed by 500Å of graded n^+ InGaAs ($0<x<1$), with the surface being terminated in InAs ($x=1$). The as deposited source/drain contacts showed ohmic behavior without requiring post-deposition heat treatment and yielded specific contact resistivity values as low as $1x10^{-6}$ Ω-cm^2. In addition these contacts were shown to be thermally stable and retained excellent surface morphology up to 600° C. The resulting all-refractory FET devices exhibited excellent dc transistor characteristics with measured peak transconductance of 140 mS/mm and a pinch-off voltage of -2.2V. Results on the high temperature reliability of these devices will also be reported. Furthermore, the performance and reliability of these devices will be compared with conventional FETs fabricated on similar material structures but which use the standard AuGe/Ni/Au ohmic metallization system.

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